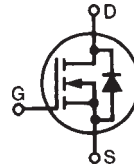


# PolarHV™ HiPerFET Power MOSFET

N-Channel Enhancement Mode  
Avalanche Rated  
Fast Intrinsic Diode

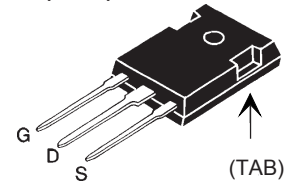
**IXFH 44N50P**  
**IXFK 44N50P**  
**IXFT 44N50P**



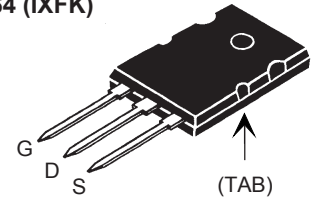
$V_{DSS} = 500 \text{ V}$   
 $I_{D25} = 44 \text{ A}$   
 $R_{DS(on)} \leq 140 \text{ m}\Omega$   
 $t_{rr} \leq 200 \text{ ns}$

Symbol	Test Conditions	Maximum Ratings	
$V_{DSS}$	$T_J = 25^\circ\text{C}$ to $175^\circ\text{C}$	500	V
$V_{DGR}$	$T_J = 25^\circ\text{C}$ to $175^\circ\text{C}$ ; $R_{GS} = 1 \text{ M}\Omega$	500	V
$V_{GSM}$	Transient	$\pm 40$	V
$V_{GSM}$	Continuous	$\pm 30$	V
$I_{D25}$	$T_C = 25^\circ\text{C}$	44	A
$I_{DM}$	$T_C = 25^\circ\text{C}$ , pulse width limited by $T_{JM}$	110	A
$I_{AR}$	$T_C = 25^\circ\text{C}$	44	A
$E_{AR}$	$T_C = 25^\circ\text{C}$	55	mJ
$E_{AS}$	$T_C = 25^\circ\text{C}$	1.7	J
$dv/dt$	$I_S \leq I_{DM}$ , $di/dt \leq 100 \text{ A}/\mu\text{s}$ , $V_{DD} \leq V_{DSS}$ , $T_J \leq 150^\circ\text{C}$ , $R_G = 10 \Omega$	10	V/ns
$P_D$	$T_C = 25^\circ\text{C}$	650	W
$T_J$		-55 ... +150	$^\circ\text{C}$
$T_{JM}$		150	$^\circ\text{C}$
$T_{stg}$		-55 ... +150	$^\circ\text{C}$
$T_L$	1.6 mm (0.062 in.) from case for 10 s	300	$^\circ\text{C}$
$T_{SOLD}$	Plastic case for 10 s	260	$^\circ\text{C}$
$M_d$	Mounting torque (TO-247)	1.13/10	Nm/lb.in.
Weight	TO-247	6	g
	TO-268	5	g
	TO-264	10	g

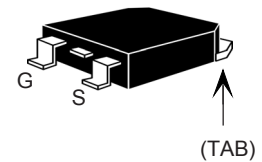
TO-247 AD (IXFH)



TO-264 (IXFK)



TO-268 (IXFT)



G = Gate      D = Drain  
S = Source      TAB = Drain

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
$BV_{DSS}$	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$	500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 4 \text{ mA}$	3.0		5.0 V
$I_{GSS}$	$V_{GS} = \pm 30 \text{ V}_{DC}$ , $V_{DS} = 0$			$\pm 10 \text{ nA}$
$I_{DSS}$	$V_{DS} = V_{DSS}$			25 $\mu\text{A}$
	$V_{GS} = 0 \text{ V}$ $T_J = 125^\circ\text{C}$			500 $\mu\text{A}$
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$ , $I_D = 0.5 I_{D25}$ Pulse test, $t \leq 300 \mu\text{s}$ , duty cycle $d \leq 2\%$			140 $\text{m}\Omega$

## Features

- † International standard packages
- † Unclamped Inductive Switching (UIS) rated
- † Low package inductance  
- easy to drive and to protect

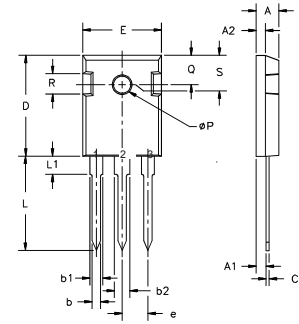
## Advantages

- † Easy to mount
- † Space savings
- † High power density

Symbol	Test Conditions	Characteristic Values ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)		
		Min.	Typ.	Max.
$g_{fs}$	$V_{DS} = 20\text{ V}$ ; $I_D = 0.5 I_{D25}$ , pulse test	20	32	S
$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$		5440	pF
$C_{oss}$			639	pF
$C_{rss}$			40	pF
$t_{d(on)}$	$V_{GS} = 10\text{ V}$ , $V_{DS} = 0.5 V_{DSS}$ , $I_D = I_{D25}$ $R_G = 3\ \Omega$ (External)		28	ns
$t_r$			29	ns
$t_{d(off)}$			85	ns
$t_f$			27	ns
$Q_{g(on)}$	$V_{GS} = 10\text{ V}$ , $V_{DS} = 0.5 V_{DSS}$ , $I_D = 0.5 I_{D25}$		98	nC
$Q_{gs}$			35	nC
$Q_{gd}$			30	nC
$R_{thJC}$				$0.19^\circ\text{C/W}$
$R_{thCS}$	(TO-247)	0.21		$^\circ\text{C/W}$
	(TO-264)	0.15		$^\circ\text{C/W}$

Symbol	Test Conditions	Characteristic Values ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)		
		Min.	Typ.	Max.
$I_s$	$V_{GS} = 0\text{ V}$			44 A
$I_{SM}$	Repetitive			110 A
$V_{SD}$	$I_F = I_s$ , $V_{GS} = 0\text{ V}$ , Pulse test, $t \leq 300\ \mu\text{s}$ , duty cycle $d \leq 2\%$			1.5 V
$t_{rr}$	$I_F = 25\text{ A}$ , $-di/dt = 100\text{ A}/\mu\text{s}$ $V_R = 100\text{ V}$ , $V_{GS} = 0\text{ V}$		0.6	200 ns
$Q_{RM}$			6.0	$\mu\text{C}$
$I_{RM}$				A

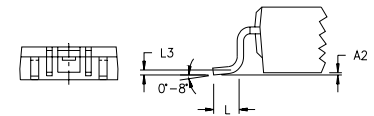
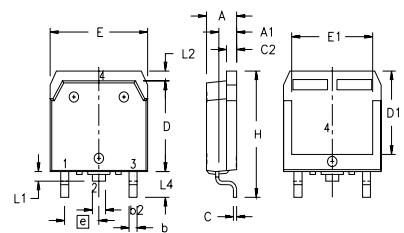
**TO-247 (IXFH) Outline**



Terminals: 1 - Gate  
2 - Drain  
3 - Source  
Tab - Drain

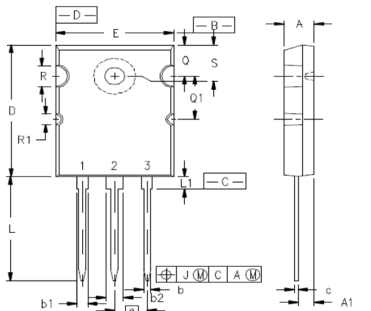
Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.7	5.3	.185	.209
A <sub>1</sub>	2.2	2.54	.087	.102
A <sub>2</sub>	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b <sub>1</sub>	1.65	2.13	.065	.084
b <sub>2</sub>	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L <sub>1</sub>		4.50		.177
∅P	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15	BSC	242	BSC

**TO-268 (IXFT) Outline**



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.001	.010	0.02	0.25
b	.045	.057	1.15	1.45
b2	.075	.083	1.90	2.10
C	.016	.026	0.40	0.65
C2	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D1	.488	.500	12.40	12.70
E	.624	.632	15.85	16.05
E1	.524	.535	13.30	13.60
e	.215 BSC		5.45 BSC	
H	.736	.752	18.70	19.10
L	.094	.106	2.40	2.70
L1	.047	.055	1.20	1.40
L2	.039	.045	1.00	1.15
L3	.010 BSC		0.25 BSC	
L4	.150	.161	3.80	4.10

**TO-264 (IXFK) Outline**



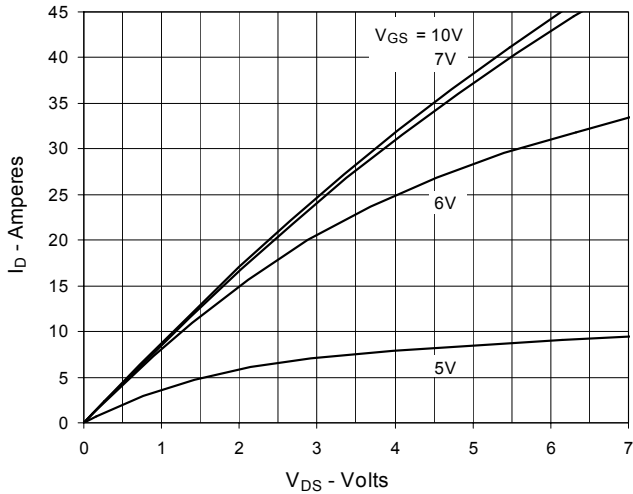
SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.209	4.70	5.31
A1	.102	.118	2.59	3.00
b	.037	.055	0.94	1.40
b1	.087	.102	2.21	2.59
b2	.110	.126	2.79	3.20
c	.017	.029	0.43	0.74
D	1.007	1.047	25.58	26.59
E	.760	.799	19.30	20.29
e	.215 BSC		5.46 BSC	
J	.000	.010	0.00	0.25
K	.000	.010	0.00	0.25
L	.779	.842	19.79	21.39
L1	.087	.102	2.21	2.59
∅P	.122	.138	3.10	3.51
Q	.240	.256	6.10	6.50
Q1	.330	.346	8.38	8.79
∅R	.155	.187	3.94	4.75
∅R1	.085	.093	2.16	2.36
S	.243	.253	6.17	6.43

BACK SIDE  
1 - GATE  
2, 4 - DRAIN (COLLECTOR)  
3 - SOURCE (EMITTER)

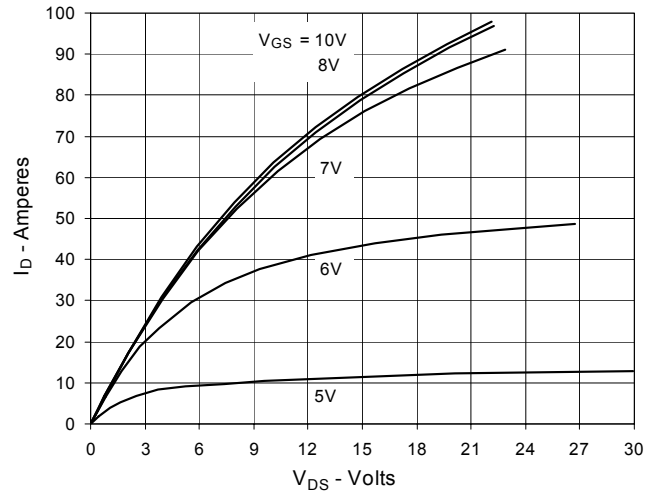
IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585  
one or more of the following U.S. patents: 4,850,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692  
4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2

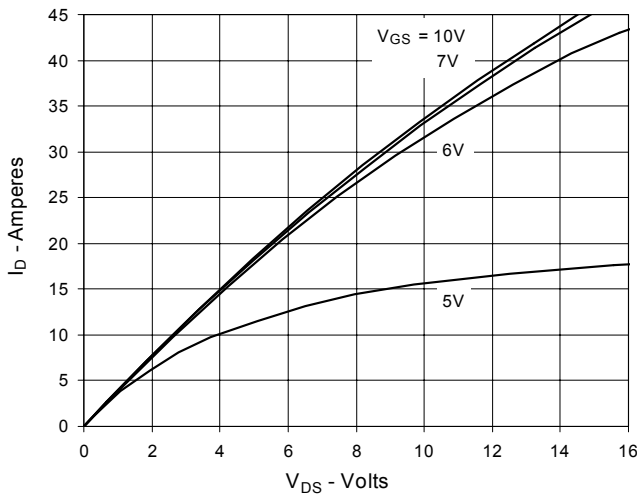
**Fig. 1. Output Characteristics @ 25°C**



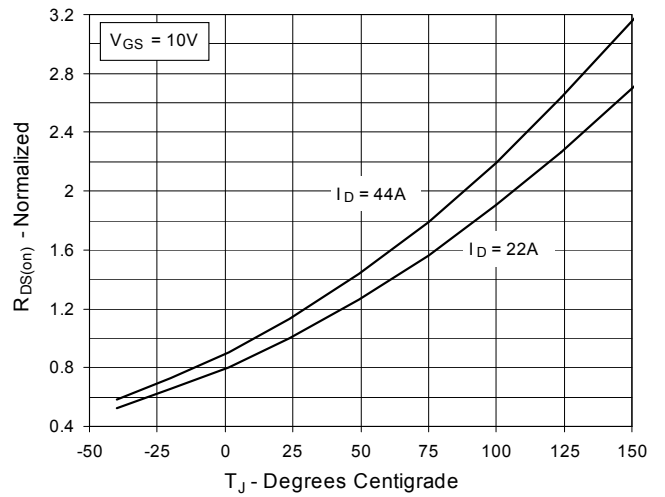
**Fig. 2. Extended Output Characteristics @ 25°C**



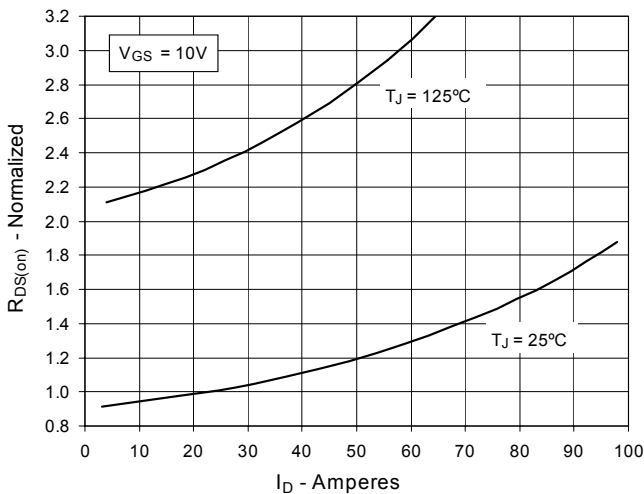
**Fig. 3. Output Characteristics @ 125°C**



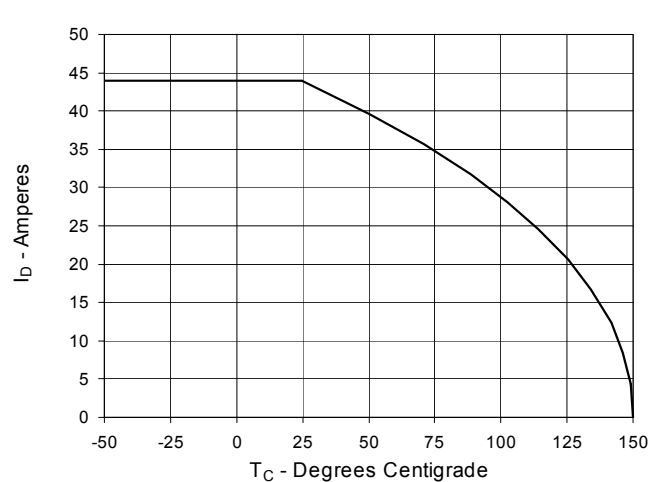
**Fig. 4.  $R_{DS(on)}$  Normalized to  $I_D = 22A$  Value vs. Junction Temperature**



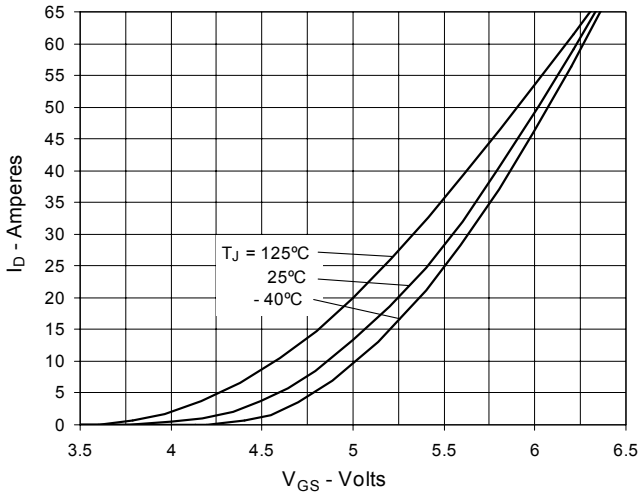
**Fig. 5.  $R_{DS(on)}$  Normalized to  $I_D = 22A$  Value vs. Drain Current**



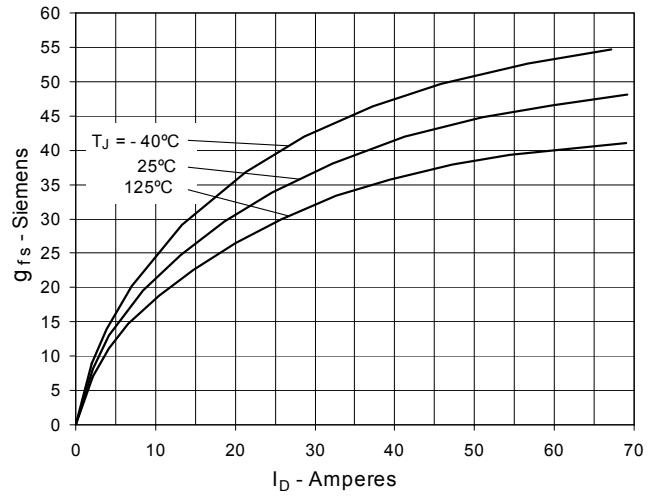
**Fig. 6. Maximum Drain Current vs. Case Temperature**



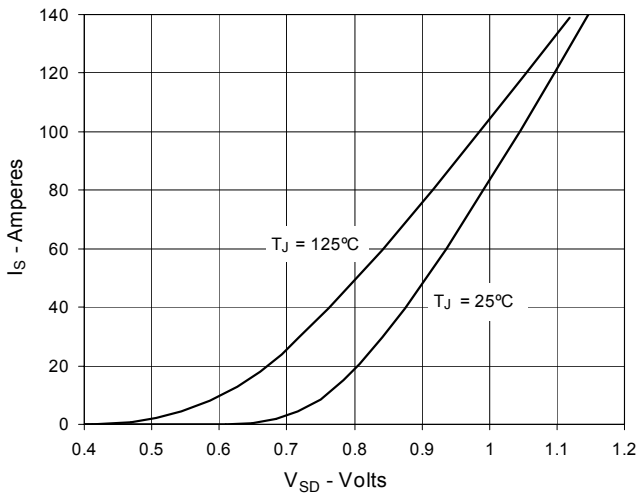
**Fig. 7. Input Admittance**



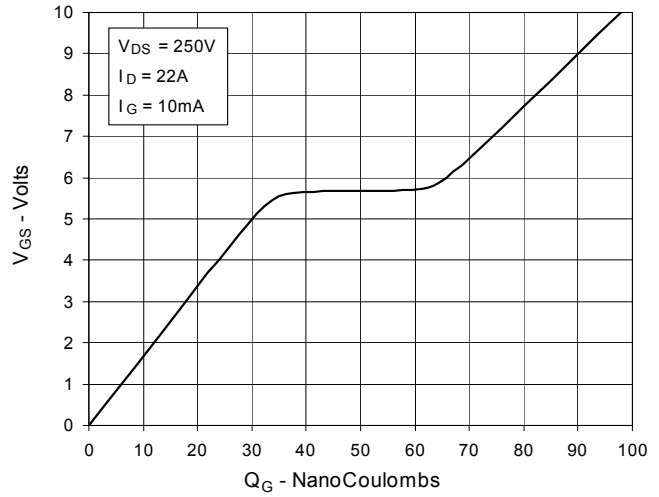
**Fig. 8. Transconductance**



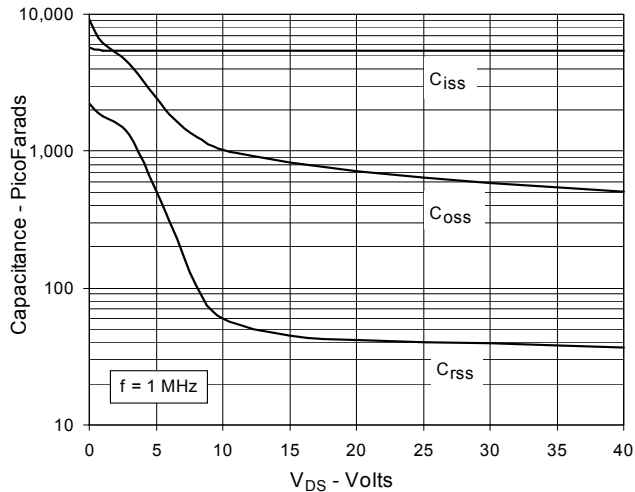
**Fig. 9. Forward Voltage Drop of Intrinsic Diode**



**Fig. 10. Gate Charge**



**Fig. 11. Capacitance**



**Fig. 12. Forward-Bias Safe Operating Area**

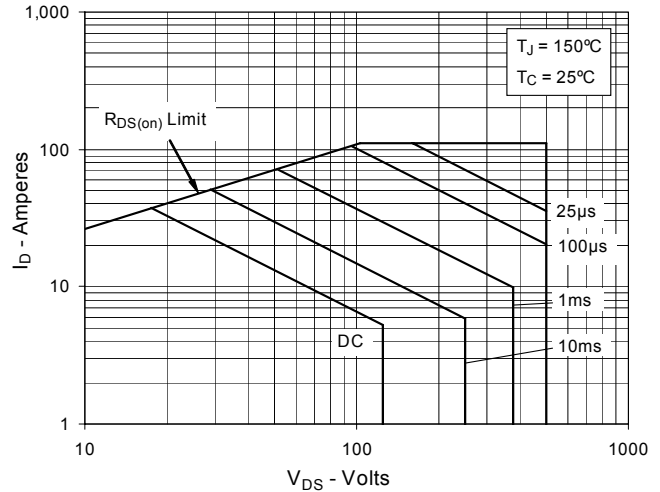


Fig. 13. Maximum Transient Thermal Resistance

