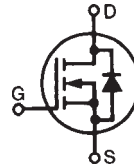


PolarHV™ HiPerFET Power MOSFET

N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode

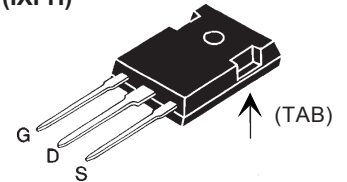
IXFH 20N80P
IXFT 20N80P
IXFV 20N80P
IXFV 20N80PS



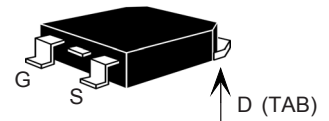
$V_{DSS} = 800 \text{ V}$
 $I_{D25} = 20 \text{ A}$
 $R_{DS(on)} \leq 520 \text{ m}\Omega$
 $t_{rr} \leq 250 \text{ ns}$

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	800	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1 \text{ M}\Omega$	800	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	$T_C = 25^\circ\text{C}$	20	A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	50	A
I_{AR}	$T_C = 25^\circ\text{C}$	10	A
E_{AR}	$T_C = 25^\circ\text{C}$	30	mJ
E_{AS}	$T_C = 25^\circ\text{C}$	1.0	J
dv/dt	$I_S \leq I_{DM}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$, $R_G = 4 \Omega$	10	V/ns
P_D	$T_C = 25^\circ\text{C}$	500	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering	300	$^\circ\text{C}$
T_{SOLD}	Plastic case for 10 s	260	$^\circ\text{C}$
M_d	Mounting torque (TO-247)	1.13/10 Nm/lb.in.	
F_C	Mounting force (PLUS220)	1.65 / 2.5..15	N/lb
Weight	TO-247	6	g
	TO-268	5.5	g
	PLUS220 types	4	g

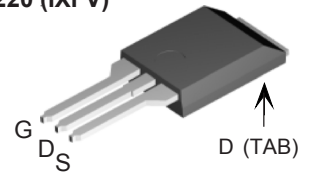
TO-247 (IXFH)



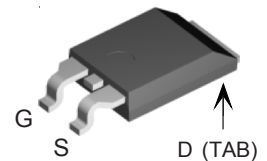
TO-268 (IXFT)



PLUS220 (IXFV)



PLUS220 SMD (IXFV..S)



G = Gate D = Drain
S = Source Tab = Drain

Features

- ¹ International standard packages
- ¹ Fast recovery diode
- ¹ Unclamped Inductive Switching (UIS) rated
- ¹ Low package inductance
- easy to drive and to protect

Advantages

- ¹ Easy to mount
- ¹ Space savings
- ¹ High power density

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	800		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 4 \text{ mA}$	3.0		5.0 V
I_{GSS}	$V_{GS} = \pm 30 \text{ V}_{DC}$, $V_{DS} = 0$			$\pm 200 \text{ nA}$
I_{DSS}	$V_{DS} = V_{DSS}$			25 μA
	$V_{GS} = 0 \text{ V}$			1000 μA
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$ Pulse test, $t \leq 300 \mu\text{s}$, duty cycle $d \leq 2 \%$			520 $\text{m}\Omega$

Symbol	Test Conditions	Characteristic Values		
		(T _J = 25°C unless otherwise specified)		
		Min.	Typ.	Max.
g_{fs}	V _{DS} = 20 V; I _D = 10 A, pulse test	14	23	S
C_{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz		4685	pF
C_{oss}			356	pF
C_{rss}			26	pF
t_{d(on)}	V _{GS} = 10 V, V _{DS} = 0.5 V _{DSS} , I _D = 10 A R _G = 2 Ω (External)		30	ns
t_r			24	ns
t_{d(off)}			85	ns
t_f			24	ns
Q_{g(on)}	V _{GS} = 10 V, V _{DS} = 0.5 V _{DSS} , I _D = 10 A		86	nC
Q_{gs}			27	nC
Q_{gd}			24	nC
R_{thJC}	(TO-247, PLUS220)		0.25	°CW
R_{thCS}			0.21	°CW

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values		
		(T _J = 25°C unless otherwise specified)		
		Min.	Typ.	Max.
I_S	V _{GS} = 0 V			20 A
I_{SM}	Repetitive			50 A
V_{SD}	I _F = I _S , V _{GS} = 0 V, Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %			1.5 V
t_{rr}	I _F = 25A, -di/dt = 100 A/μs V _R = 100V; V _{GS} = 0 V			250 ns
Q_{RM}			0.8	μC
I_{RM}			6.0	A

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2

Fig. 1. Output Characteristics
@ 25°C

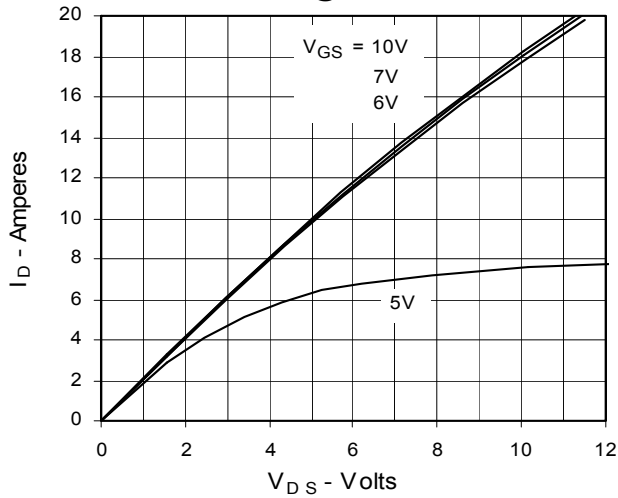


Fig. 2. Extended Output Characteristics
@ 25°C

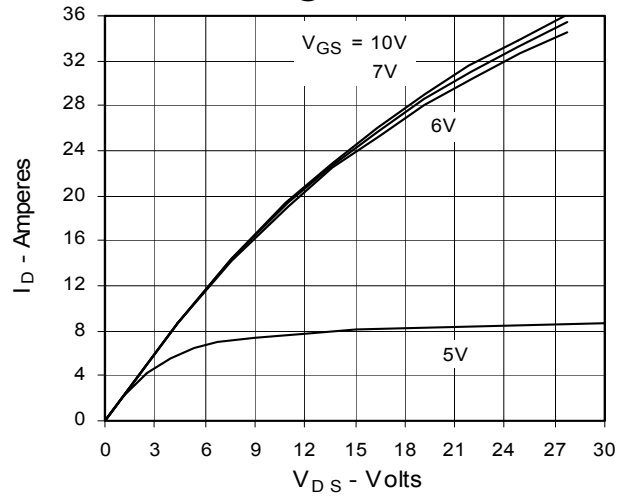


Fig. 3. Output Characteristics
@ 125°C

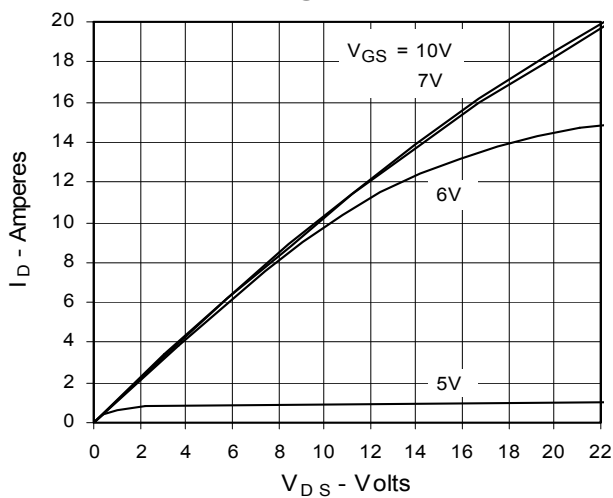


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 10A$ Value vs. Junction Temperature

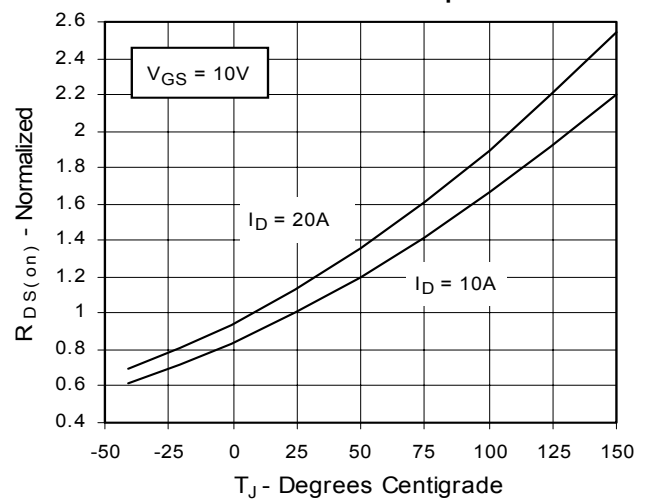


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 10A$ Value vs. Drain Current

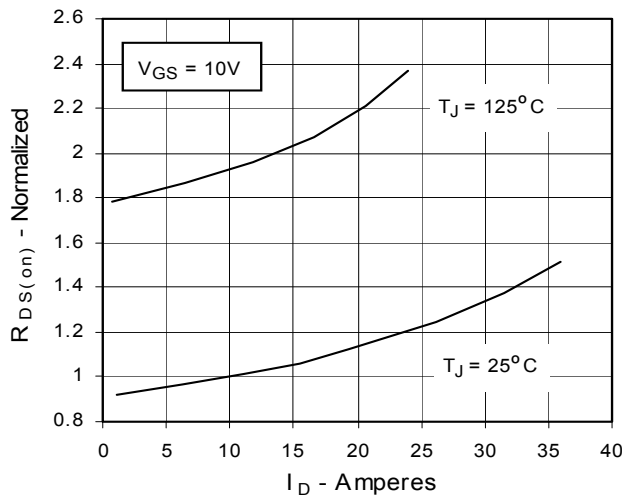


Fig. 6. Drain Current vs. Case Temperature

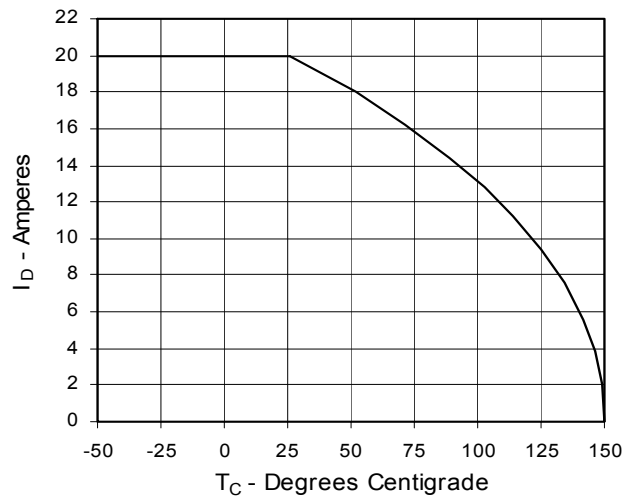


Fig. 7. Input Admittance

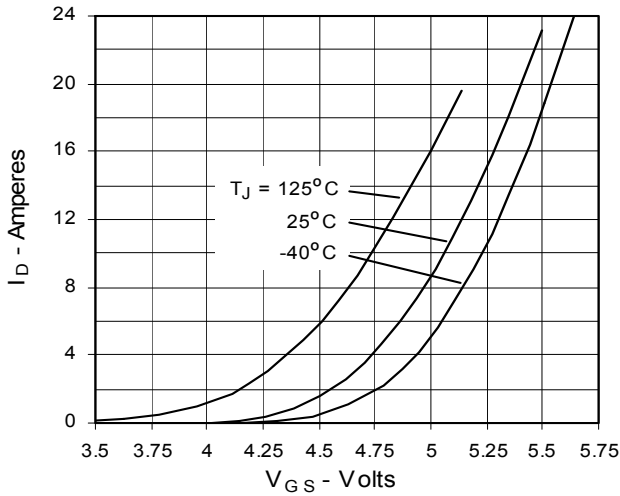


Fig. 8. Transconductance

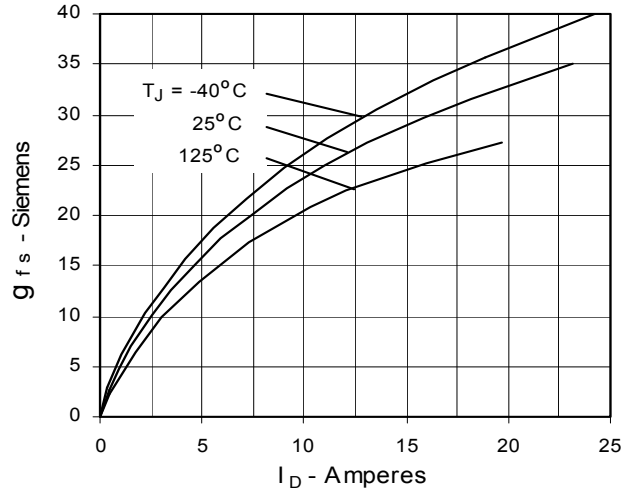


Fig. 9. Source Current vs. Source-To-Drain Voltage

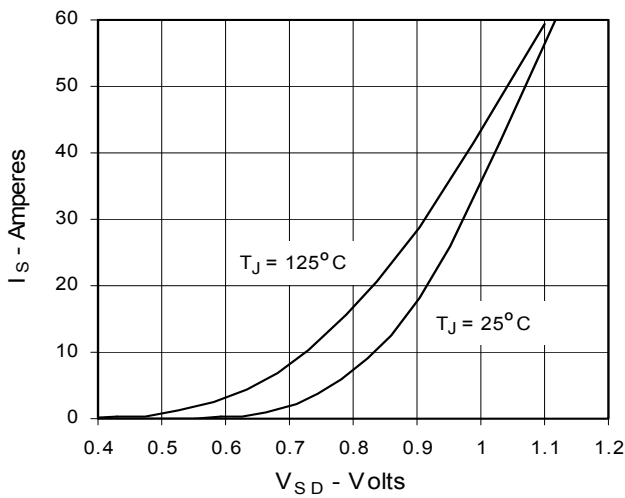


Fig. 10. Gate Charge

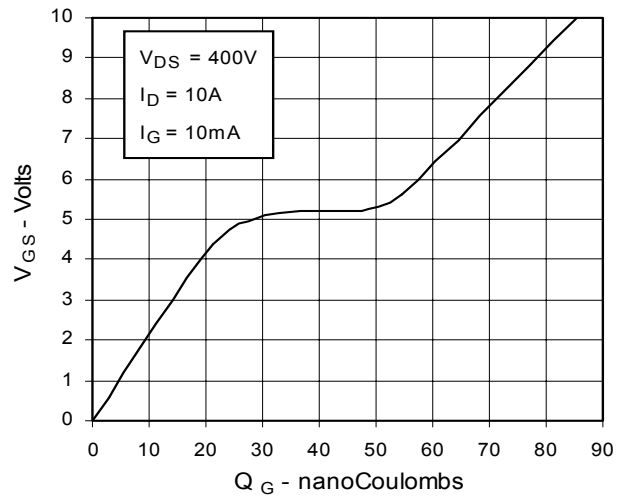


Fig. 11. Capacitance

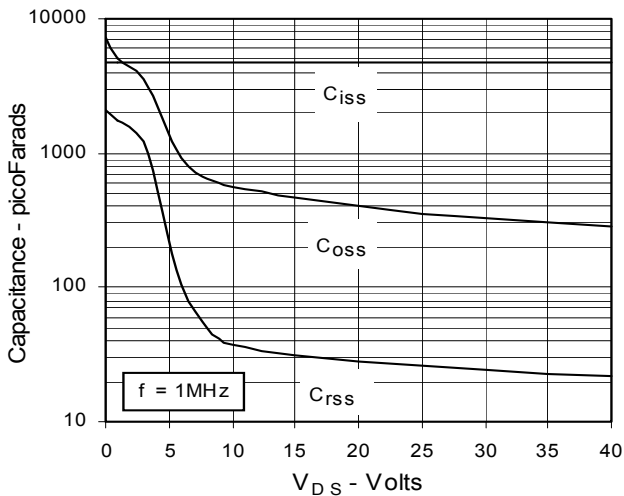
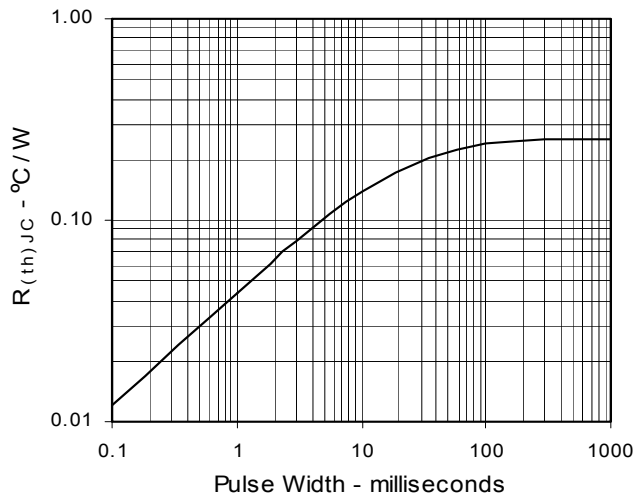


Fig. 12. Maximum Transient Thermal Resistance



Package Outline Drawings

