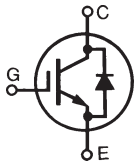
High Voltage IGBT with Diode

(Electrically Isolated Back Surface)

IXGR 35N120BD1

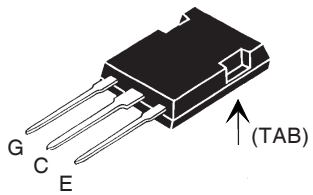
V_{CES} = 1200 V
I_{C25} = 54 A
$V_{CE(sat)}$ = 3.5 V
$t_{fi(typ)}$ = 160 ns



Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	1200	V
V_{CGR}	T_J = 25°C to 150°C; R_{GE} = 1 MΩ	1200	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C	54	A
I_{C110}	T_C = 110°C	28	A
I_{F110}	T_C = 110°C	8	A
I_{CM}	T_C = 25°C, 1 ms	200	A
SSOA (RBSOA)	V_{GE} = 15 V, T_J = 125°C, R_G = 10 Ω Clamped inductive load	I_{CM} = 120 @0.8 V_{CES}	A
P_C	T_C = 25°C	250	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
V_{ISOL}	50/60 Hz, RMS, t = 1 min I_{SOL} = 1mA, t = 1 s	2500 3000	V~ V~
F_C	Mounting force	22...130/5...29	N/lb
	Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s	300	°C
Weight		6	g

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)		Characteristic Values min.	typ.	max.	
$V_{GE(th)}$	I_C = 250 µA, V_{CE} = V_{GE}		2.5		5.0	V
I_{CES}	V_{CE} = V_{CES} V_{GE} = 0 V	T=25°C T=125°C			50 250	µA µA
I_{GES}	V_{CE} = 0 V, V_{GE} = ±20 V				±100	nA
$V_{CE(sat)}$	I_C = 35A, V_{GE} = 15 V Note 2			2.8	3.5	V

ISOPLUS247 (IXGR)



G = Gate C = Collector
E = Emitter TAB = Electrically Isolated

Features

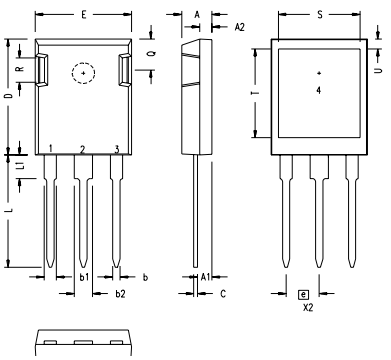
- Silicon chip on DCB substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- IGBT and anti-parallel FRED for resonant power supplies
  - Induction heating
  - Rice cookers
- MOS Gate turn-on
  - drive simplicity
- Fast Recovery Expitaxial Diode (FRED)
  - soft recovery with low I_{RM}

Advantages

- Saves space (two devices in one package)
- Easy to mount
- Reduces assembly time and cost

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	I_C = 35A; V_{CE} = 10 V, Note 2.	28	38		S
C_{ies}			2300		pF
C_{oes}	V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz		190		pF
C_{res}			80		pF
Q_g			140		nC
Q_{ge}	I_C = 40A, V_{GE} = 15 V, V_{CE} = 0.5 V_{CES}		20		nC
Q_{gc}			50		nC
$t_{d(on)}$	**Inductive load, T_J = 25°C**		40		ns
t_{ri}	I_C = 35 A; V_{GE} = 15 V		50		ns
E_{on}	V_{CE} = 0.8 V_{CES}; R_G = R_{off} = 3 Ω		0.9		mJ
$t_{d(off)}$	Note 1.		270	500	ns
t_{fi}			160	300	ns
E_{off}			3.8	7.0	mJ
$t_{d(on)}$	**Inductive load, T_J = 125°C**		45		ns
t_{ri}	I_C = 35A; V_{GE} = 15 V		60		ns
E_{on}	V_{CE} = 0.8 V_{CES}; R_G = R_{off} = 3 Ω		1.9		mJ
$t_{d(off)}$	Note 1		380		ns
t_{fi}			400		ns
E_{off}			8.0		mJ
R_{thJC}				0.5	K/W
R_{thCK}			0.25		K/W

ISOPLUS247 Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

Reverse Diode (FRED)

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_F	I_F = 10 A, V_{GE} = 0 V			3.3	V
	I_F = 10 A, V_{GE} = 0 V, T_J = 125°C			2.2	V
I_{RM}	I_F = 10 A; -di_F/dt = 100 A/µs, V_R = 100 V		4.0		A
t_{rr}	V_{GE} = 0 V; T_J = 125°C		190		ns
t_{rr}	I_F = 1 A; -di_F/dt = 100 A/µs; V_R = 30 V, V_{GE} = 0 V		40		ns
R_{thJC}				2.5	K/W

Notes: 1. Switching times may increase for V_{CE} (Clamp) > 0.8 • V_{CES}, higher T_J or increased R_G.
2. Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %.