

High Voltage Power MOSFET

IXTH02N250 IXTV02N250S

$$V_{DSS} = 2500V$$

$$I_{D25} = 200mA$$

$$R_{DS(on)} \leq 450\Omega$$

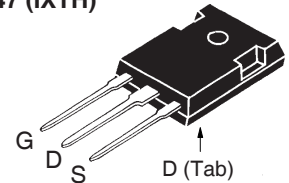
N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode



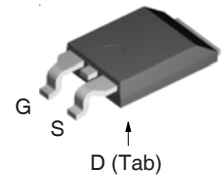
Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	2500	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C , $R_{GS} = 1M\Omega$	2500	V
V_{GSS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ\text{C}$	200	mA
I_{DM}	$T_C = 25^\circ\text{C}$, Pulse Width Limited by T_{JM}	400	mA
P_D	$T_C = 25^\circ\text{C}$	57	W
T_J		- 55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		- 55 ... +150	$^\circ\text{C}$
T_L	1.6mm (0.062 in.) from Case for 10s	300	$^\circ\text{C}$
T_{SOLD}	Plastic Body for 10s	260	$^\circ\text{C}$
M_d	Mounting Torque	1.13 / 10	Nm/lb.in
F_c	Mounting Force	11..65 / 25..14.6	N/lb.
Weight	PLUS220	4	g
	TO-247	6	g

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 250\mu\text{A}$	2500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	2.0		4.0 V
I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$			± 100 nA
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$ $T_J = 125^\circ\text{C}$			5 μA 50 μA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 50\text{mA}$, Note 1			450 Ω

TO-247 (IXTH)



PLUS220SMD (IXTV_S)



G = Gate D = Drain
S = Source Tab = Drain

Features

- Avalanche Rated
- Fast Intrinsic Diode
- Low Package Inductance

Advantages

- Easy to Mount
- Space Savings

Applications

- High Voltage Power Supplies
- Capacitor Discharge
- Pulse Circuits

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 100\text{V}$, $I_D = 0.5 \cdot I_{D25}$, Note 1	88	145	mS
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		120	pF
C_{oss}			9	pF
C_{rss}			3	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$ $R_G = 100\Omega$ (External)		19	ns
t_r			19	ns
$t_{d(off)}$			32	ns
t_f			33	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$		6.6	nC
Q_{gs}			0.4	nC
Q_{gd}			4.9	nC
R_{thJC}			2.2	$^\circ\text{C/W}$
R_{thCS}		0.25		$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_s	$V_{GS} = 0\text{V}$			200 mA
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			800 mA
V_{SD}	$I_F = 100\text{mA}$, $V_{GS} = 0\text{V}$, Note 1			2.5 V
t_{rr}	$I_F = 200\text{mA}$, $-di/dt = 50\text{A}/\mu\text{s}$, $V_R = 100\text{V}$		1.5	μs

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

*Additional provisions for lead to lead voltage isolation are required at $V_{DS} > 1200\text{V}$.

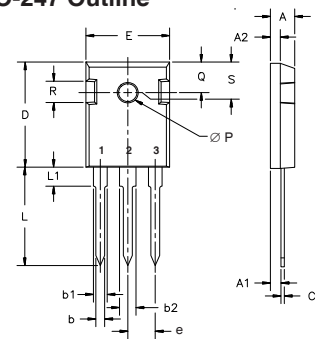
PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338B2
by one or more of the following U.S. patents: 4,850,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2
4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

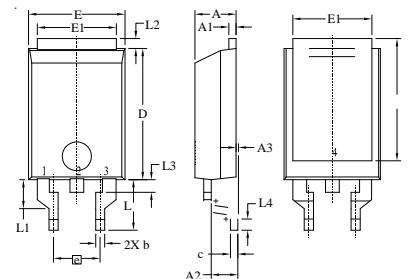
TO-247 Outline



Terminals: 1 - Gate 2 - Drain
3 - Source Tab - Drain

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.7	5.3	.185	.209
A ₁	2.2	2.54	.087	.102
A ₂	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b ₁	1.65	2.13	.065	.084
b ₂	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
∅P	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216

PLUS220SMD Outline



1. Gate 2. Drain
3. Source 4. Drain

SYM	INCHES		MILLIMETER	
	MIN	MAX	MIN	MAX
A	.169	.185	4.30	4.70
A1	.028	.035	0.70	0.90
A2	.098	.118	2.50	3.00
A3	.000	.010	0.00	0.25
b	.035	.047	0.90	1.20
b1	.080	.095	2.03	2.41
b2	.054	.064	1.37	1.63
c	.028	.035	0.70	0.90
D	.551	.591	14.00	15.00
D1	.512	.539	13.00	13.70
E	.394	.433	10.00	11.00
E1	.331	.346	8.40	8.80
e	.200BSC		5.08 BSC	
L	.209	.228	5.30	5.80
L1	.118	.138	3.00	3.50
L2	.035	.051	0.90	1.30
L3	.045	.053	1.25	1.35
L4	.039	.059	1.00	1.50

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

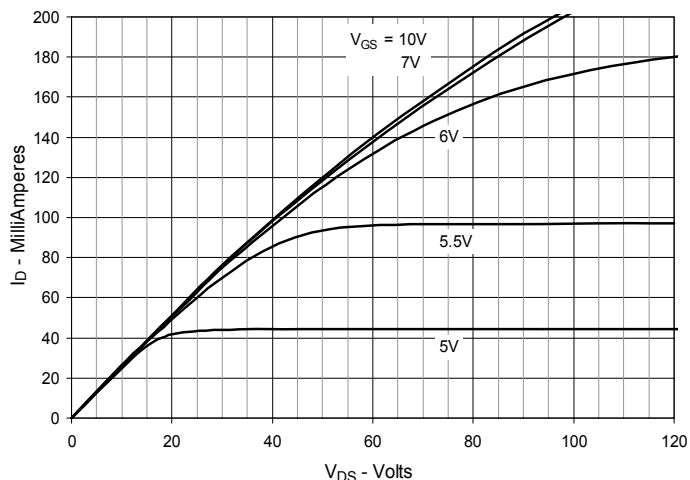


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

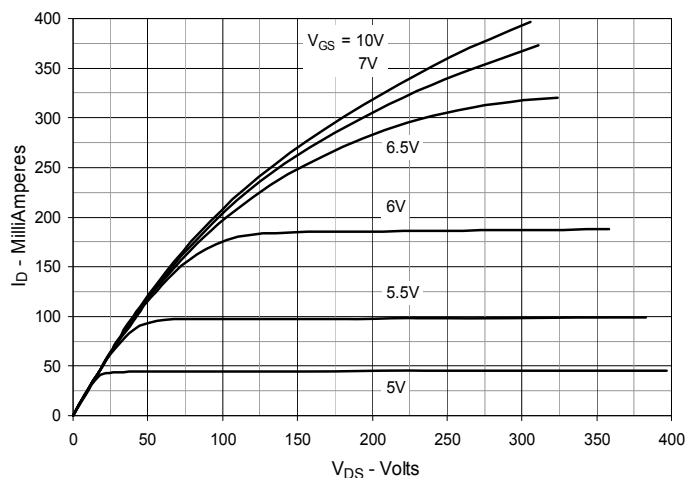


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

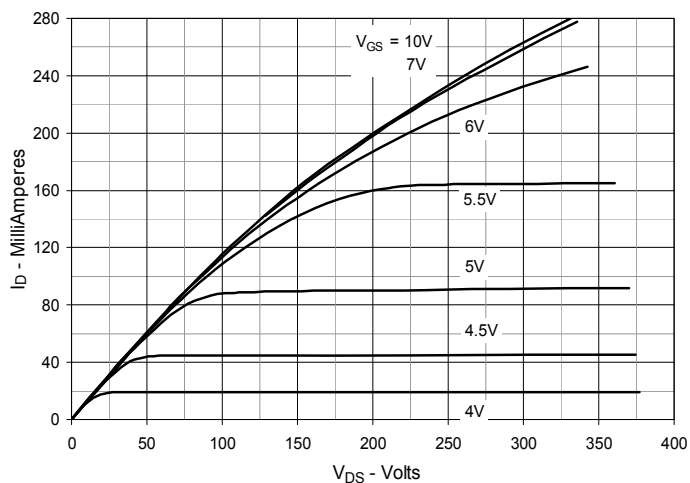


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 100\text{mA}$ Value vs. Junction Temperature

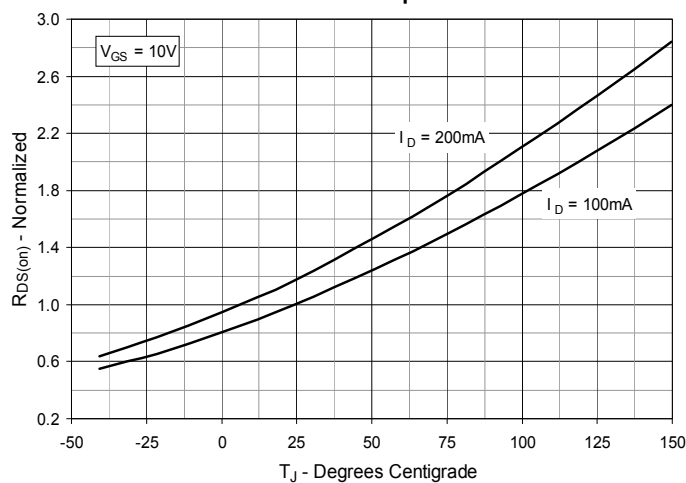


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 100\text{mA}$ Value vs. Drain Current

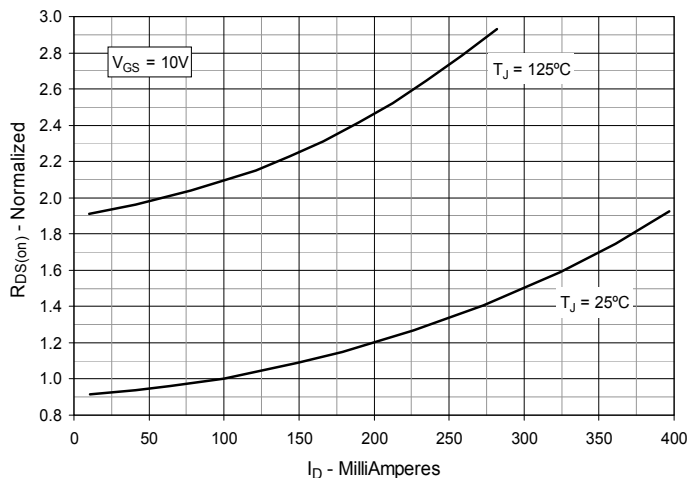


Fig. 6. Maximum Drain Current vs. Case Temperature

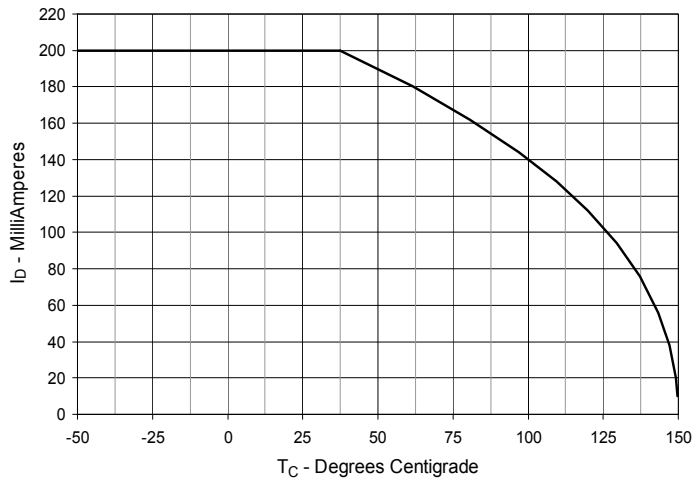


Fig. 7. Input Admittance

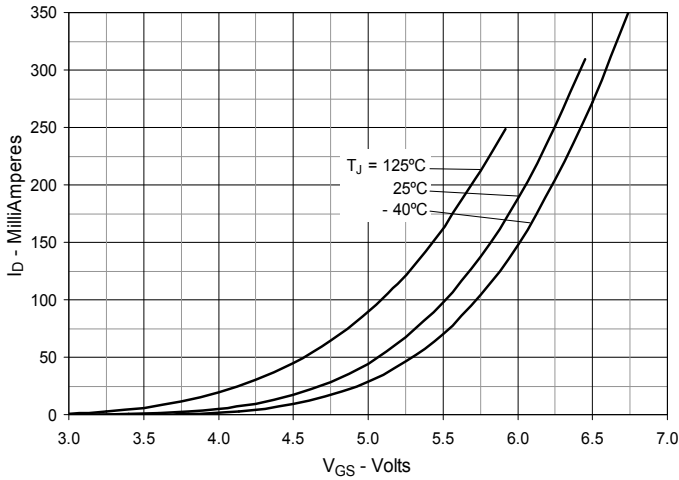


Fig. 8. Transconductance

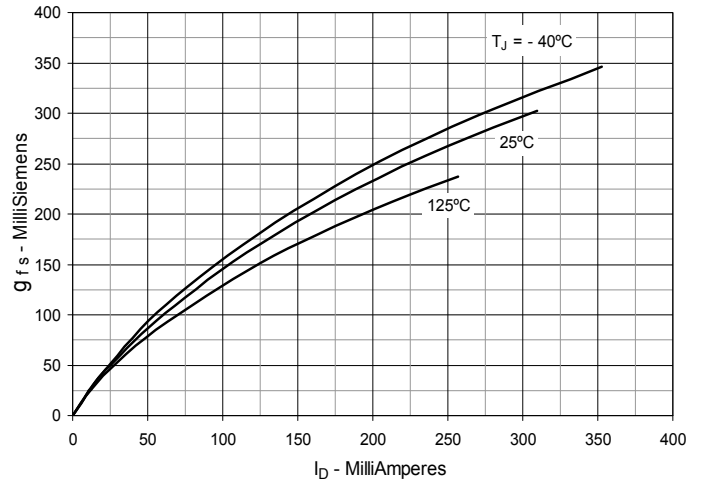


Fig. 9. Forward Voltage Drop of Intrinsic Diode

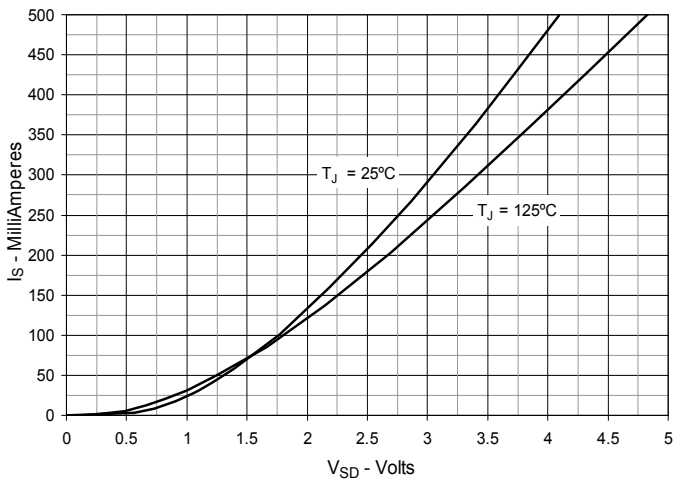


Fig. 10. Gate Charge

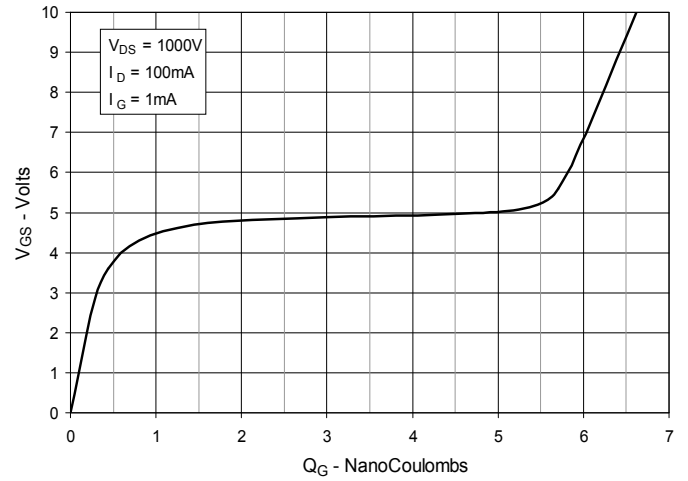


Fig. 11. Capacitance

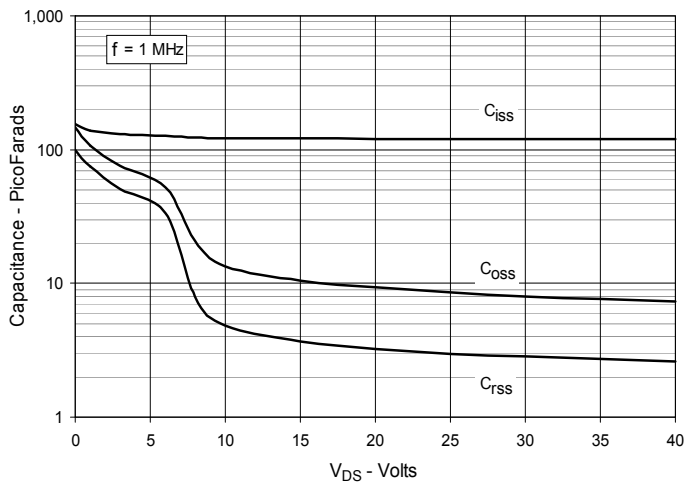


Fig. 12. Maximum Transient Thermal Impedance

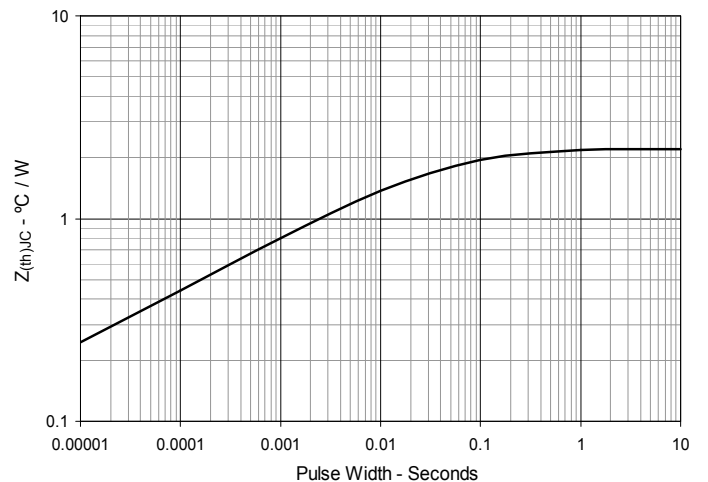


Fig. 13. Forward-Bias Safe Operating Area
@ $T_C = 25^\circ\text{C}$

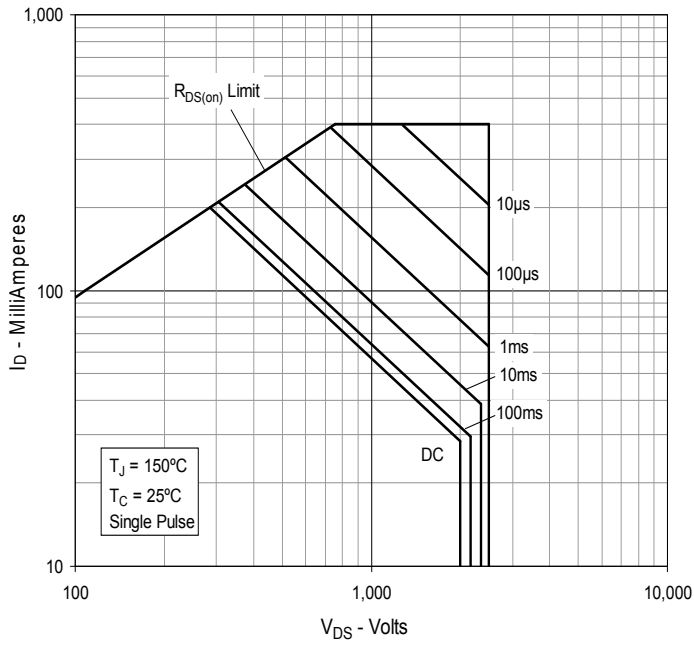


Fig. 14. Forward-Bias Safe Operating Area
@ $T_C = 75^\circ\text{C}$

